Mapping pipeline skeletons onto heterogeneous platforms

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Introduction and motivation

- Mapping applications onto parallel platforms
  Difficult challenge
- Heterogeneous clusters, fully heterogeneous platforms
  Even more difficult!
- Structured programming approach
  - Easier to program (deadlocks, process starvation)
  - Range of well-known paradigms (pipeline, farm)
  - Algorithmic skeleton: help for mapping

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- Chains-on-chains partitioning problem
  - no communications
  - identical processors
- Extensions (done)
  - with communications
  - with heterogeneous processors/links
  - goal: assess complexity, design heuristics
- Extensions (current work)
  - deal with DEALs
  - deal with DAGs

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Chains-on-chains

Load-balance contiguous tasks

5 7 3 4 8 1 3 8 2 9 7 3 5 2 3 6

- Back to Bokhari and Iqbal partitioning papers
- See survey by Pinar and Aykanat, JPDC 64, 8 (2004)

Chains-on-chains

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- Map each pipeline stage on a single processor (no deals)
- Goal: minimize execution time

- Several mapping strategies

The pipeline application

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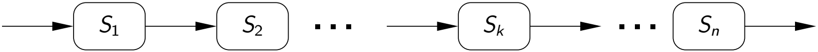

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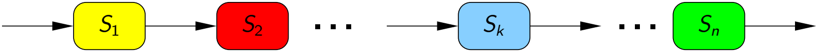

ONE-TO-ONE MAPPING

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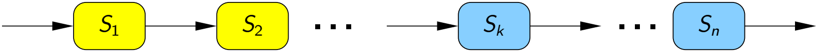

INTERVAL MAPPING

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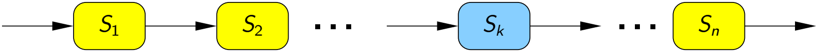

GENERAL MAPPING

Major contributions

Theory Formal approach to the problem
Problem complexity
Integer linear program for exact resolution

Practice Heuristics for INTERVAL MAPPING on clusters
Experiments to compare heuristics and evaluate their absolute performance

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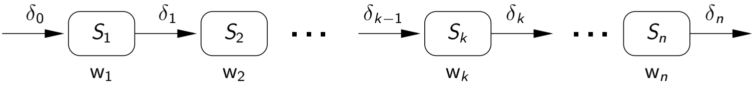
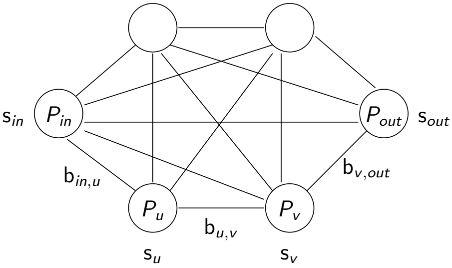


- n stages $\mathcal{S}_k$, $1 \leq k \leq$ n
- $\mathcal{S}_k$:
  - receives input of size δ_{k-1} from $\mathcal{S}_{k-1}$
  - performs w_k computations
  - outputs data of size δ_k to $\mathcal{S}_{k+1}$
- $\mathcal{S}_0$ and $\mathcal{S}_{n+1}$: virtual stages representing the outside world

The platform



- p processors P_u, $1 \leq u \leq$ p, fully interconnected
- s_u: speed of processor P_u
- bidirectional link $\text{link}_{u,v} : P_u \rightarrow P_v$, bandwidth $b_{u,v}$
- one-port model: each processor can either send, receive or compute at any time-step
- P_{in}: input data – P_{out}: output data

Different platforms

Fully Homogeneous – Identical processors ($s_u = s$) and links ($b_{u,v} = b$): typical parallel machines

Communication Homogeneous – Different-speed processors ($s_u \neq s_v$), identical links ($b_{u,v} = b$): networks of workstations, clusters

Fully Heterogeneous – Fully heterogeneous architectures, $s_u \neq s_v$ and $b_{u,v} \neq b_{u',v'}$: hierarchical platforms, grids

Mapping problem: One-to-one Mapping

- n $\leq$ p: map each stage $\mathcal{S}_k$ onto a distinct processor $P_{\text{alloc}(k)}$
- Period of $P_{\text{alloc}(k)}$: minimum delay between processing of two consecutive tasks

$$\longrightarrow \boxed{S_{k-1}} \longrightarrow \boxed{S_k} \longrightarrow \boxed{S_{k+1}} \longrightarrow$$

$t = \text{alloc}(k-1)$ $\quad$ $u = \text{alloc}(k)$ $\quad$ $v = alloc(k+1)$

- Cycle-time of P_u: $cycle_u = \frac{\delta_{k-1}}{\mathsf{b}_{t,u}} + \frac{\mathsf{w}_k}{\mathsf{s}_u} + \frac{\delta_k}{\mathsf{b}_{u,v}}$
- Optimization problem: find the allocation function alloc : $[1, \text{n}] \rightarrow [1, \text{p}]$ which minimizes

$$T_{\text{period}} = \max_{1 \leq k \leq \text{n}} cycle_{\text{alloc}(k)}$$

(with alloc(0) = *in* and alloc(n + 1) = *out*)

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Mapping problem: INTERVAL MAPPING

- Several consecutive stages onto the same processor
- Increase computational load, reduce communications
- Mandatory when p < n
- Partition of [1..n] into m intervals $I_j = [d_j, e_j]$ (with $d_j \leq e_j$ for $1 \leq j \leq m$, $d_1 = 1$, $d_{j+1} = e_j + 1$ for $1 \leq j \leq m-1$ and $e_m = \mathrm{n}$)
- Interval I_j mapped onto processor $P_{\mathrm{alloc}(j)}$

$$T_{\mathrm{period}} = \max_{1 \leq j \leq m} \left\{ \frac{\delta_{d_j - 1}}{\mathrm{b}_{\mathrm{alloc}(j-1),\mathrm{alloc}(j)}} + \frac{\sum_{i=d_j}^{e_j} \mathrm{w}_i}{\mathrm{s}_{\mathrm{alloc}(j)}} + \frac{\delta_{e_j}}{\mathrm{b}_{\mathrm{alloc}(j),\mathrm{alloc}(j+1)}} \right\}$$

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Mapping problem: GENERAL MAPPING

- Not suiting the one-port model very well: can always be replaced by an INTERVAL MAPPING as good as the general one for *Communication Homogeneous* platforms
- Can be the optimal mapping for *Fully Heterogeneous* platforms in some particular cases
- More general, but requires threads and may lead to idle times and races with the one-port model

Outline

Complexity results

	Fully Hom.	Comm. Hom.
One-to-one Mapping		
Interval Mapping		
General Mapping		

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- Binary search polynomial algorithm for ONE-TO-ONE MAPPING
- Dynamic programming algorithm for INTERVAL MAPPING on Hom. platforms
- General mapping: same complexity as INTERVAL MAPPING
- All problem instances NP-complete on *Fully Heterogeneous* platforms

Back to chains-on-chains

- Chains-on-chains + homogeneous communications: polynomial ☺
- Chains-on-chains + different-speed processors: NP-complete ☹

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One-to-one/Comm. Hom.: binary search algorithm

- Work with fastest n processors, numbered P_1 to P_n, where $\mathrm{s}_1 \leq \mathrm{s}_2 \leq \ldots \leq \mathrm{s}_\mathrm{n}$
- Mark all stages $\mathcal{S}_1$ to $\mathcal{S}_\mathrm{n}$ as free
- **For** $u = 1$ **to** n
  - Pick up any free stage $\mathcal{S}_k$ s.t. $\delta_{k-1}/\mathrm{b} + \mathrm{w}_k/\mathrm{s}_u + \delta_k/\mathrm{b} \leq T_\mathrm{period}$
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Interval, Fully Hom.: dynamic programming algorithm

- $c(i,j,k)$: optimal period to map stages S_i to S_j using exactly k processors
- Goal: $\min_{1 \leq k \leq \mathrm{p}} c(1, \mathrm{n}, k)$

$$c(i,j,k) = \min_{\substack{q+r=k \\ 1 \leq q \leq k-1 \\ 1 \leq r \leq k-1}} \left\{ \min_{i \leq \ell \leq j-1} \{\max(c(i,\ell,q), c(\ell+1,j,r))\} \right\}$$

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- Proof: search over all possible partitionings into two subintervals, using every possible number of processors for each interval
- Complexity: $O(\mathrm{n}^3\mathrm{p}^2)$

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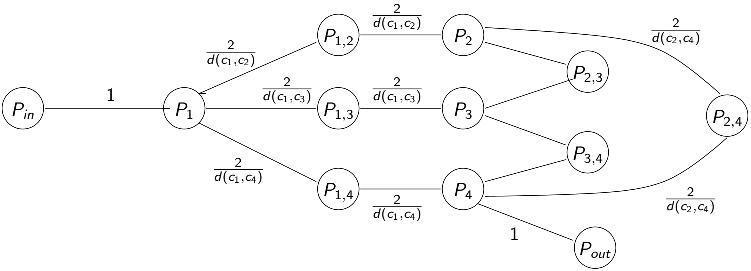
Heterogeneous platforms: NP-complete

- Reduction from MINIMUM METRIC BOTTLENECK WANDERING SALESPERSON PROBLEM



Outline

Greedy heuristics (1/2)

- Target clusters: *Communication Homogeneous* platforms and INTERVAL MAPPING
- $L = \lceil n/p \rceil$ consecutive stages per processor: set of intervals fixed
- $\lceil n/L \rceil$ processors used
- ONE-TO-ONE MAPPING when $n \leq p$ ($L = 1$)
- Rule applied in all greedy heuristics except random interval length

Greedy heuristics (2/2)

H1a-GR: random – Random choice of a free processor for each interval

H1b-GRIL: random interval length – Idem with random interval sizes: average length L, $1 \leq \text{length} \leq 2L-1$

H2-GSW: biggest $\sum w$ – Place interval with most computations on fastest processor

H3-GSD: biggest $\delta_{in} + \delta_{out}$ – Intervals are sorted by communications $(\delta_{in} + \delta_{out})$
in: first stage of interval; $out - 1$: last one

H4-GP: biggest period on fastest processor – Balancing computation and communication: processors sorted by decreasing speed s_u; for current processor u, choose interval with biggest period $(\delta_{in} + \delta_{out})/\text{b} + \sum_{i \in Interval} w_i/s_u$

Sophisticated heuristics

H5-BS121: binary search for ONE-TO-ONE MAPPING – optimal algorithm for ONE-TO-ONE MAPPING. When $p < n$, application cut in fixed intervals of length L.

H6-SPL: splitting intervals – Processors sorted by decreasing speed, all stages to first processor. At each step, select used proc j with largest period, split its interval (give fraction of stages to j'): minimize $max(period(j), period(j'))$ and split if maximum period improved.

H7a-BSL and H7b-BSC: binary search (longest/closest) – Binary search on period P: start with stage $s = 1$, build intervals (s, s') fitting on processors. For each u, and each $s' \geq s$, compute period $(s..s', u)$ and check whether it is smaller than P. **H7a**: maximizes s'; **H7b**: chooses the closest period.

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Plan of experiments

- Assess performance of polynomial heuristics
- Random applications, $n = 1$ to 50 stages
- Random platforms, $p = 10$ and $p = 100$ processors
- $b = 10$ (comm. hom.), proc. speed between 1 and 20
- Relevant parameters: ratios $\frac{\delta}{b}$ and $\frac{w}{s}$
- Average over 100 similar random appli/platform pairs

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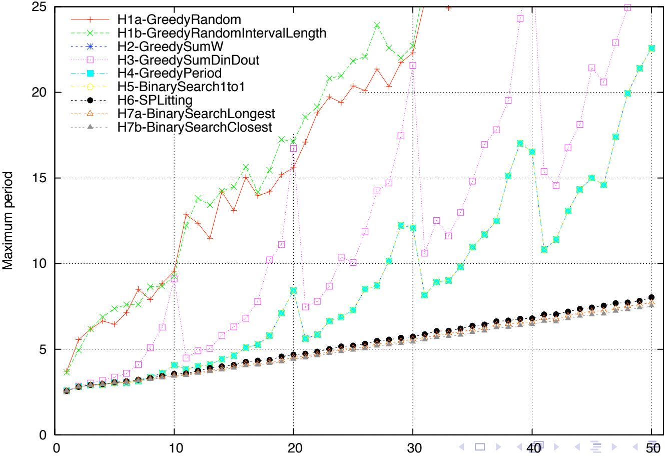

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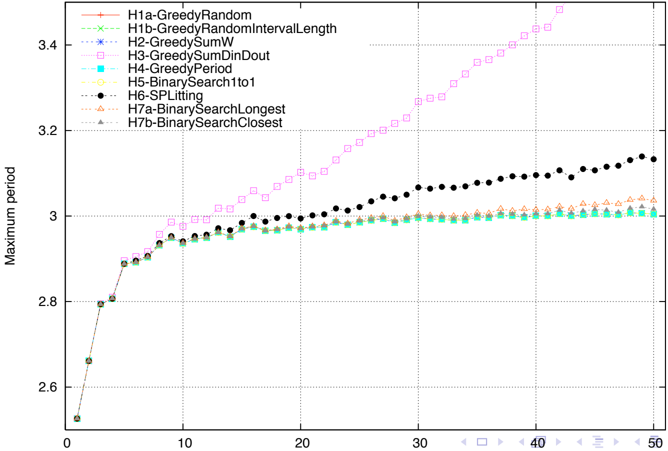

Experiment 2 - balanced comm/comp, het comm

- communication time between 1 and 100
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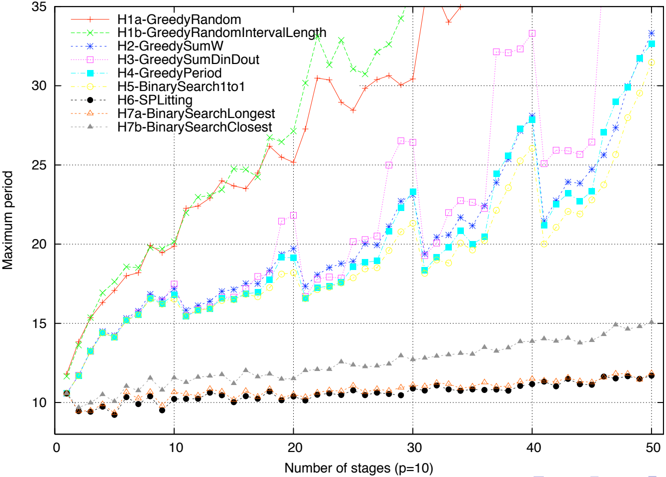

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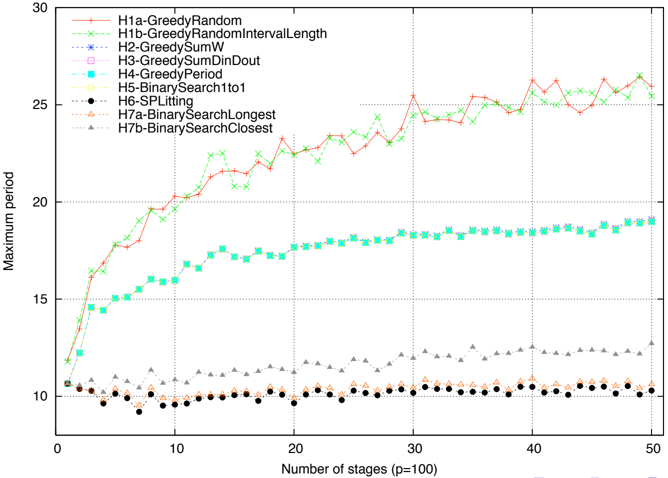

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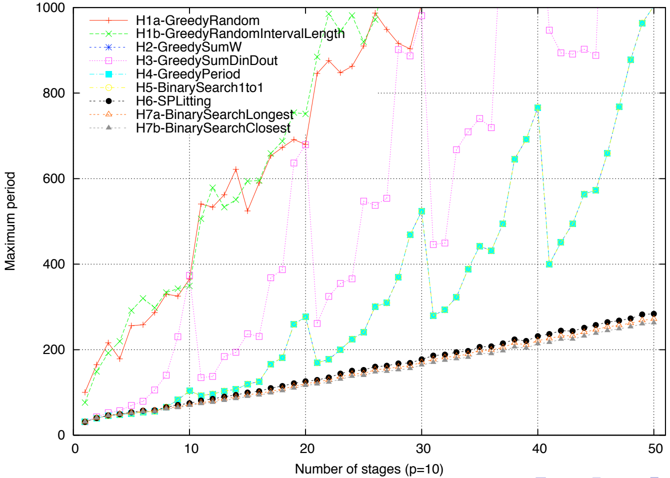

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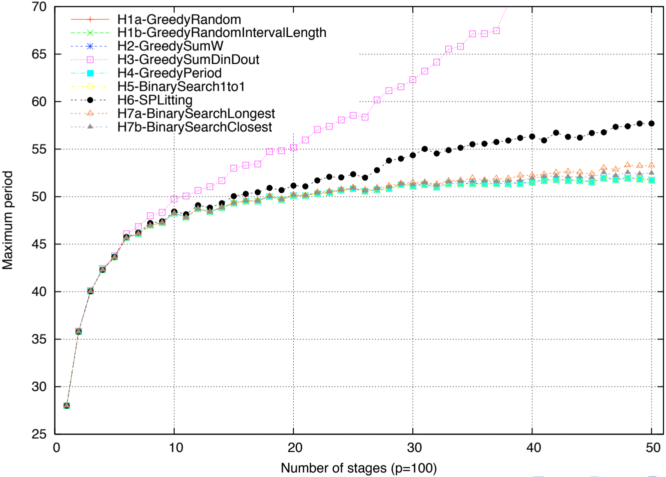

Experiment 4 - computations

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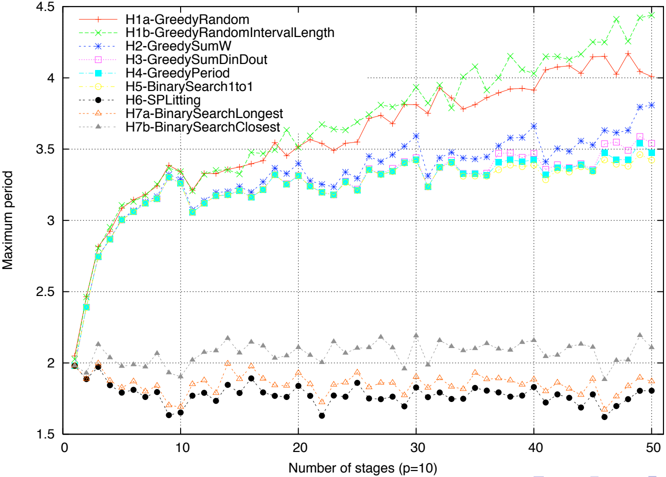

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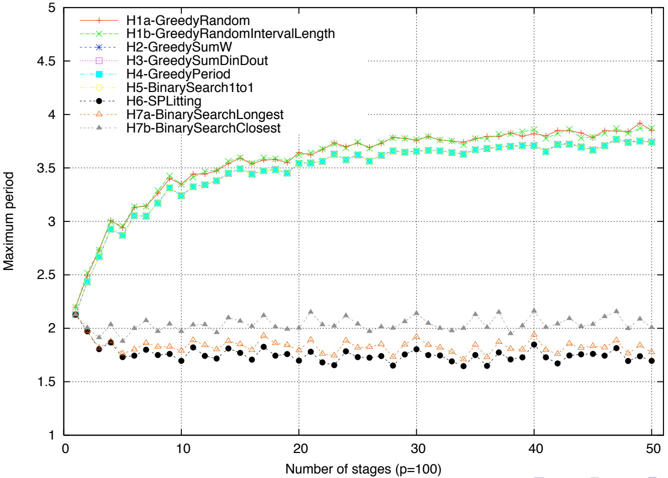

Summary of experiments

- Much more efficient than random mappings
- Three dominant heuristics for different cases
- Insignificant communications (hom. or small) and many processors: H5-BS121 (ONE-TO-ONE MAPPING)
- Insignificant communications (hom. or small) and few processors: H7b-BSC (clever choice where to split)
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Outline

Integer linear programming

- Integer LP to solve INTERVAL MAPPING on *Fully Heterogeneous* platforms
- Many integer variables: no efficient algorithm to solve
- Approach limited to small problem instances
- Absolute performance of the heuristics for such instances

Linear program: variables

- $x_{k,u}$: 1 if S_k on P_u (0 otherwise)
- $y_{k,u}$: 1 if $\mathcal{S}_k$ and S_{k+1} both on P_u (0 otherwise)
- $z_{k,u,v}$: 1 if $\mathcal{S}_k$ on P_u and S_{k+1} on P_v (0 otherwise)
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- $\forall k \in [0..\mathrm{n}+1], \quad \sum_u x_{k,u} = 1$
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- $\forall k \in [0..\mathrm{n}], \forall u, v \in [1..\mathrm{p}] \cup \{in, out\}, u \neq v, x_{k,u} + x_{k+1,v} \leq 1 + z_{k,u,v}$
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- $\forall k \in [1..\mathrm{n}], \forall u \in [1..\mathrm{p}], \quad \mathrm{last}_u \geq k.x_{k,u}$
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- $\forall k \in [1..\mathrm{n}-1], \forall u, v \in [1..\mathrm{p}], u \neq v, \quad \mathrm{first}_v \geq (k+1).z_{k,u,v}$

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- $O(np^2)$ variables, as many constraints
- Experiments only on small problem instances
- Average over 10 instances of each application

- Use GLPK
- Largest experiment: $p = 8$, $n = 4$: 14-hour computation time
- Parameters similar to Experiment 1: homogeneous communications and balanced comm/comp

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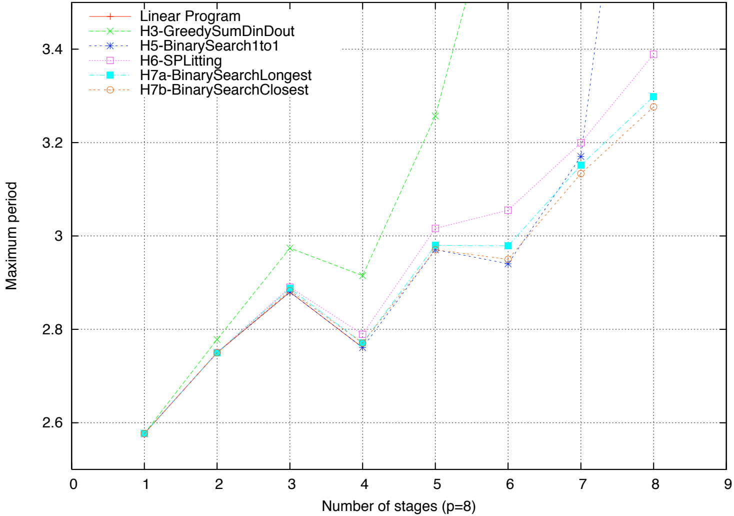
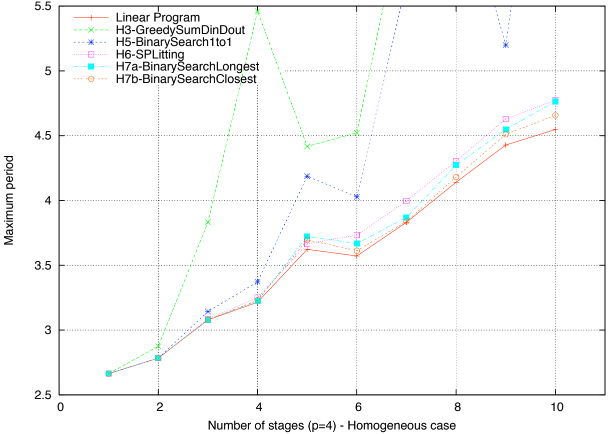


Linear program: experiment $p = 8$

n	LP	H5-BS121	H7b-BSC
1	2.576857	2.576882	2.576882
2	2.749913	2.749934	2.749934
3	2.879871	2.879900	2.883072
4	2.760960	2.760981	2.770690

Linear program: experiment p = 4

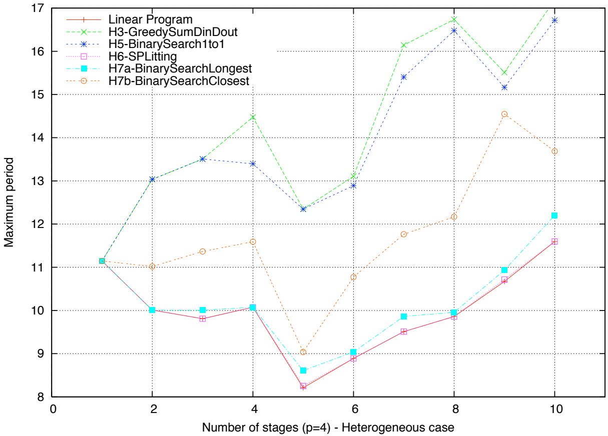
Homogeneous communications (Experiment 1)



H7b very close to the optimal ($< 3\%$ error)

Linear program: experiment $p = 4$

Heterogeneous communications (Experiment 2)



H6 very close to the optimal ($< 0.05\%$ error)

Outline

Related work

Scheduling task graphs on heterogeneous platforms– Acyclic task graphs scheduled on different speed processors [Topcuoglu et al.]. Communication contention: 1-port model [Beaumont et al.].

Mapping pipelined computations onto special-purpose architectures– FPGA arrays [Fabiani et al.]. Fault-tolerance for embedded systems [Zhu et al.]

Mapping pipelined computations onto clusters and grids– DAG [Taura et al.], DataCutter [Saltz et al.]

Mapping skeletons onto clusters and grids– Use of stochastic process algebra [Benoit et al.]

Conclusion

Theoretical side – Complexity for different mapping strategies and different platform types

Practical side

- Optimal polynomial algorithm for One-to-one Mapping
- Design of several heuristics for Interval Mapping on *Communication Homogeneous*
- Comparison of their performance
- Linear program to assess the absolute performance of the heuristics, which turns out to be quite good

Future work

Short term

- Heuristics for *Fully Heterogeneous* platforms
- Extension to DAG-trees (a DAG which is a tree when un-oriented)
- Extension to stage replication
- LP with replication and DAG-trees

Longer term

- Real experiments on heterogeneous clusters, using an already-implemented skeleton library and MPI
- Comparison of effective performance against theoretical performance